(6 pages) Reg. No. : .....

Code No. : 20121 E **Sub. Code : SACS 21/ SASE 21**

B.Sc. (CBCS) DEGREE EXAMINATION, NOVEMBER 2022.

Second Semester

Computer Science/Software Engineering – Allied

DIGITAL DESIGN

(For those who joined in July 2017–2019 onwards)

Time : Three hours Maximum : 75 marks

PART A — (10 × 1 = 10 marks)

Answer ALL questions.

Choose the correct answer :

1. The radix of the hexa-decimal number system is _____

(a) 0 (b) 2

(c) 8 (d) 16

2. The _____ gate is called any-or-all gate.

(a) NAND (b) NOR

(c) OR (d) AND

3. K-map technique provides a systematic method for simplifying

(a) multiplexers

(b) logic gates

(c) Boolean expressions

(d) None of these

4. Canonical form is a unique way of representing _____

(a) SOP

(b) Minterm

(c) Boolean Expressions

(d) POS

5. What is a multiplexer?

(a) It is a type of decoder which decodes several inputs and gives one output

(b) A multiplexer is a device which converts many signals into one

(c) It takes one input and results into many output

(d) It is a type of encoder which decodes several inputs and gives one output

6. 2's complement of 11001011 is _____

(a) 01010111 (b) 11010100

(c) 00110101 (d) 11100010

7. Register is a group of _____

(a) OR & AND gates (b) Flip-flops

(c) OR gates (d) None of these

8. When both inputs of a J-K flip-flop cycle, the output will _____

(a) Be invalid (b) Change

(c) No change (d) Toggle

9. A shift register is defined as _____

(a) The register capable of shifting information to another register

(b) The register capable of shifting information either to the right or to the left

(c) The register capable of shifting information to the right only

(d) The register capable of shifting information to the left only

10. Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.

(a) 2 (b) 5

(c) 3 (d) 4

PART B — (5 × 5 = 25 marks)

Answer ALL the questions by choosing either (a) or (b).

Each answer should not exceed 250 words.

11. (a) Convert $(101101.1101)_2$ to decimal and hexadecimal form.

Or

(b) Write about basic gates with suitable diagram.

12. (a) State and prove De Morgan's theorem.

Or

(b) Give a short note on Sum of product method.

13. (a) Neatly sketch a block diagram of Multiplexer and explain it.

Or

(b) Write short notes on 2's Complement Arithmetic.

14. (a) Explain the Logic diagram of JK flip-flop.

Or

(b) Write short notes on edge triggered D flip flop.

15. (a) Describe about Serial in - Serial out Shift (SISO) Register.

Or

(b) Give short notes on Parallel in - Serial out (PISO) Shift Register.

PART C — (5 × 8 = 40 marks)

Answer ALL questions by choosing either (a) or (b).

Each answer should not exceed 600 words.

16. (a) Convert the following:

(i) $(0.513)_{10}$ to octal

(ii) $(0.6875)_{10}$ to binary.

Or

(b) Explain logic operations with NOR and NAND Gates with neat diagram.

17. (a) State and prove De Morgan's theorem. Also Apply De Morgan's theorem for the function $((A + B + C)D)'$.

Or

(b) Describe the two canonical forms of Boolean algebra.

18. (a) Explain The Half adder? Implement the full adder using two half adders.

Or

(b) Describe the functionality of a Multiplexer and Demultiplexer.

19. (a) Explain the working of the following

(i) RS flip-flop

(ii) D flip-flop

Or

(b) Elucidate in detail about edge triggered JK flip flops.

20. (a) Elaborate in detail about types of shift registers.

Or

(b) Briefly explain universal shift register with suitable diagram.

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